CLOCK GRID SKEW REDUCTION TECHNIQUE USING BIASABLE DELAY DRIVERS

Abstract

A clock grid skew reduction technique that uses one or more biasable delay drivers to compensate for unbalanced loading and/or RC wire delay induced skew is provided. The biasable delay driver has a size that may be varied depending on a delay amount of a signal from a clock source to an input of the biasable delay driver. Depending on the delay amount, the biasable delay driver may be either sized up or sized down to modulate delay in order to reduce or eliminate skew between the clock signal at the input of the biasable delay driver and the clock signal at another point in a circuit.

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